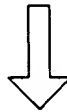


FIG. 15
PRIOR ART

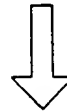
Form STI by forming openings for STI regions, filling the openings with oxide film and planarizing the surface by CMP

S11



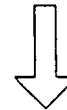
Form polysilicon gate electrode by depositing polysilicon film and etching and patterning the film

S12



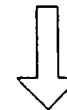
Implant p- or n-type dopant ions into substrate to define source/drain regions

S13



Silicidation

S14

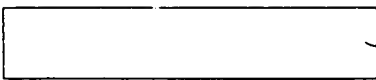


Form metal interconnects

S15



FIG. 16A
(PRIOR ART)



without dummy diffused layer with dummy diffused layer

FIG. 16B
(PRIOR ART)




FIG. 16B
(PRIOR ART)




FIG. 16C
(PRIOR ART)




FIG. 16C
(PRIOR ART)




FIG. 16D
(PRIOR ART)

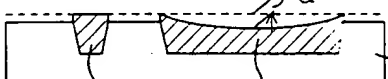
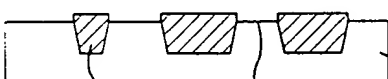


FIG. 16D
(PRIOR ART)



Process should end abnormally due to dishing

FIG. 16E
(PRIOR ART)

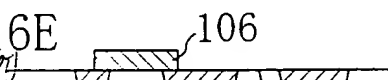


FIG. 16F
(PRIOR ART)

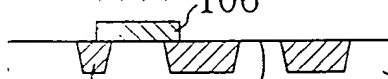


FIG. 16G
(PRIOR ART)




FIG. 17A
(PRIOR ART)

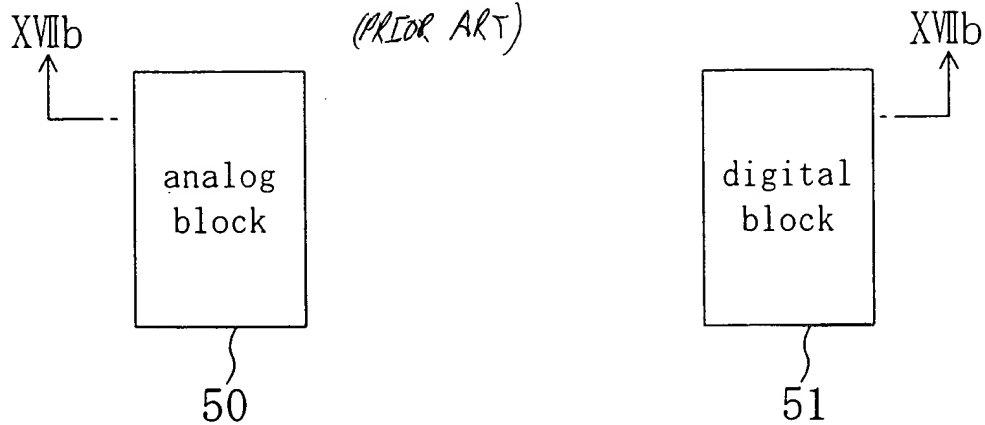


FIG. 17B
(PRIOR ART)

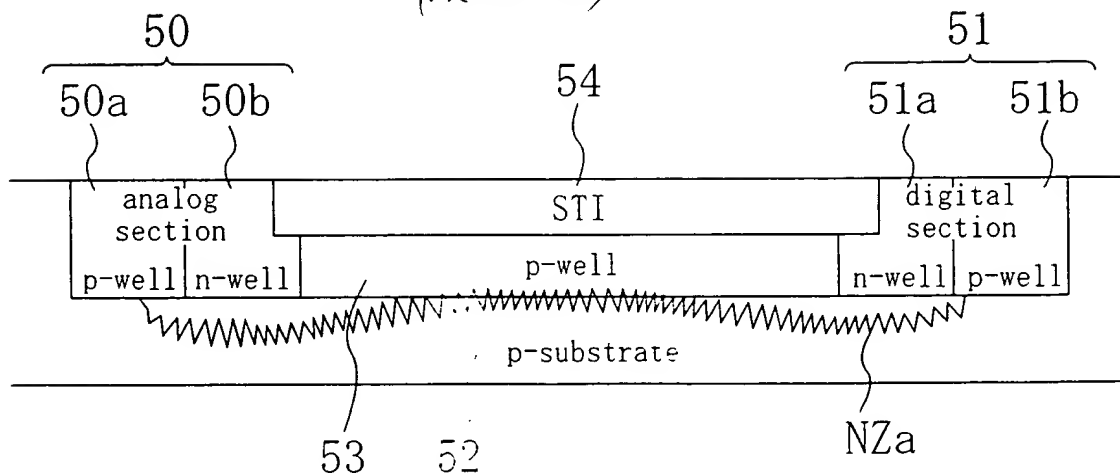




FIG. 18A
(PRIOR ART)

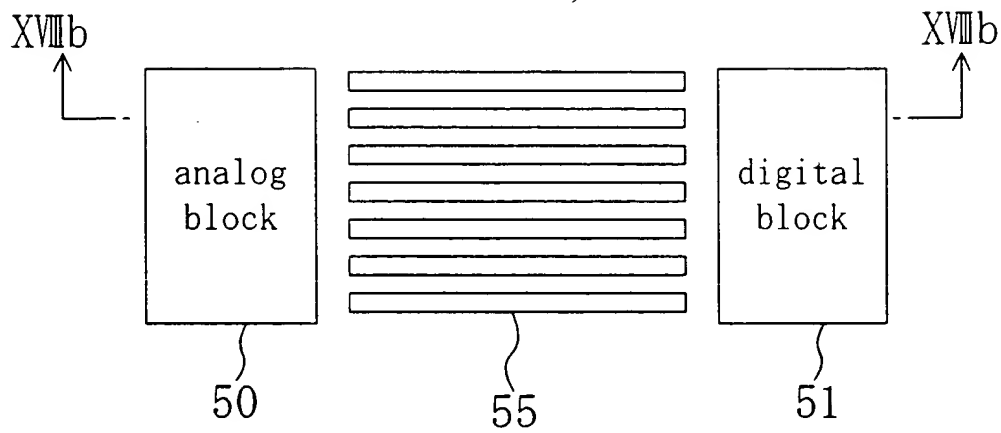


FIG. 18B
(PRIOR ART)

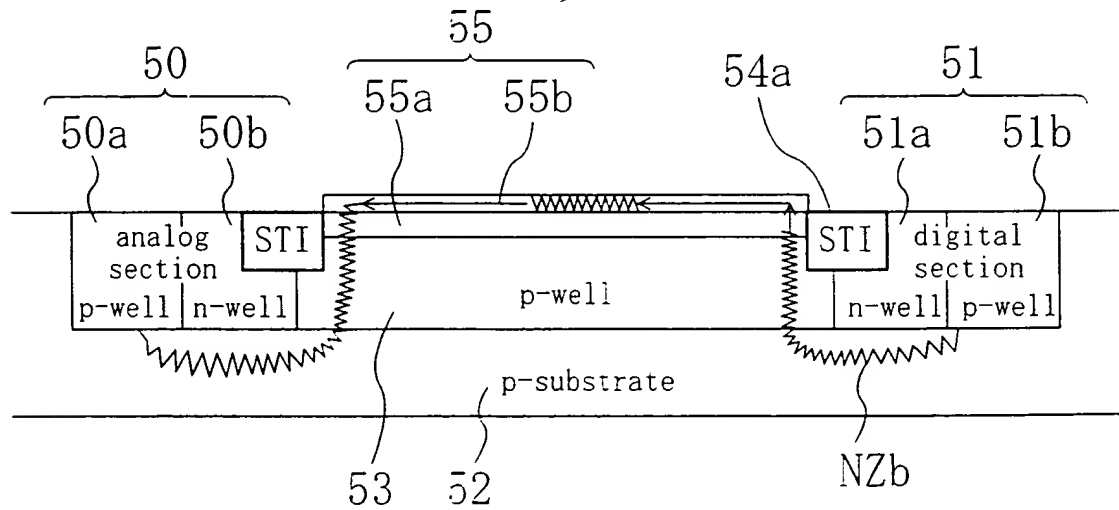




FIG. 19A
(PRIOR ART)

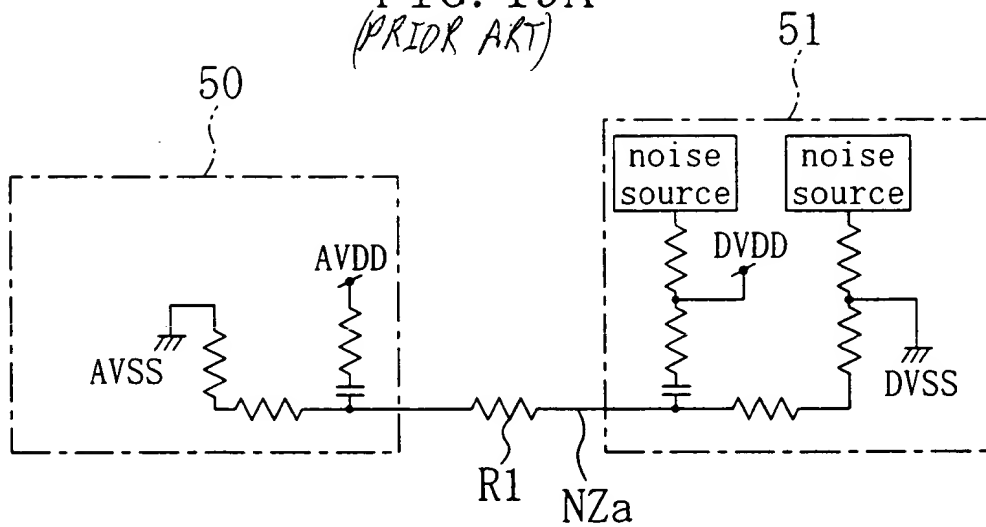


FIG. 19B
(PRIOR ART)

